

Fig. 1D

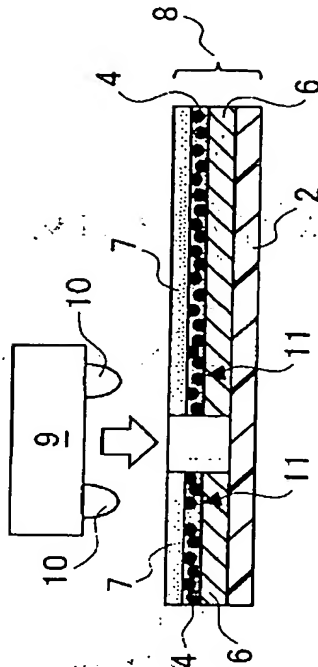
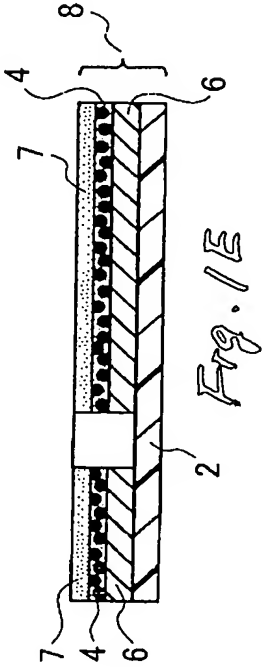


Fig. 1E

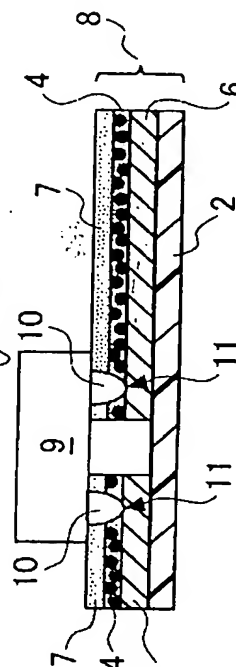


Fig. 1A

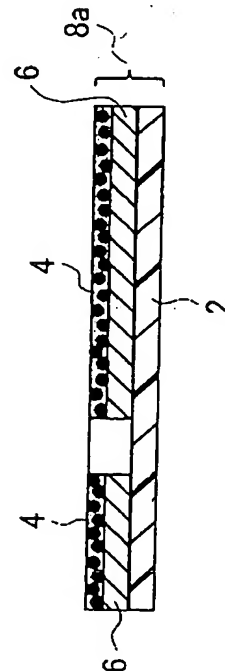
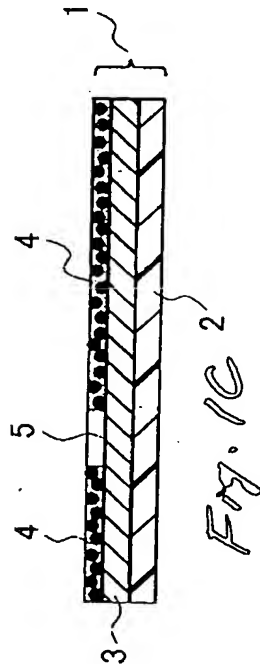
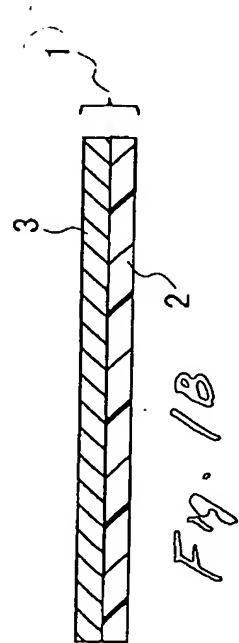


Fig. 2A

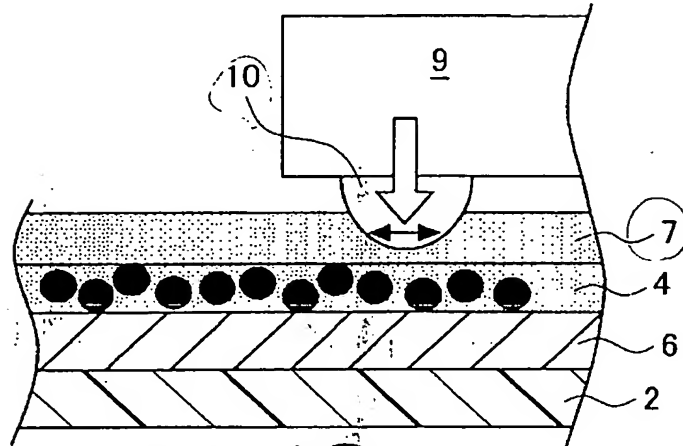


Fig. 2B

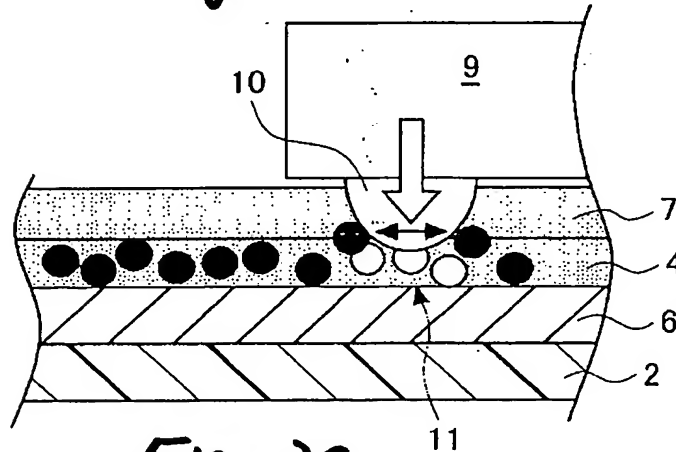


Fig. 2C

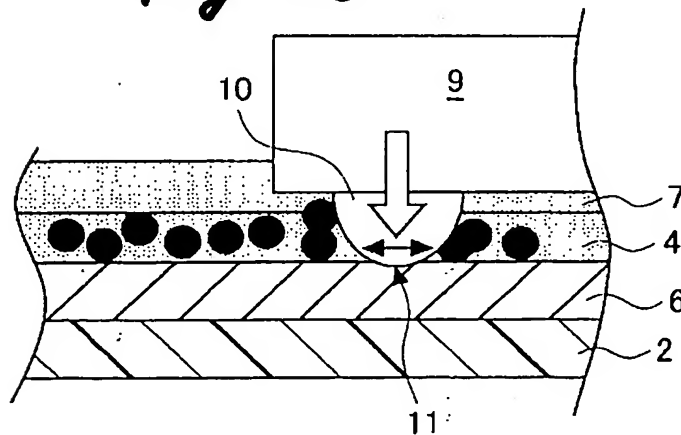


Fig. 3A

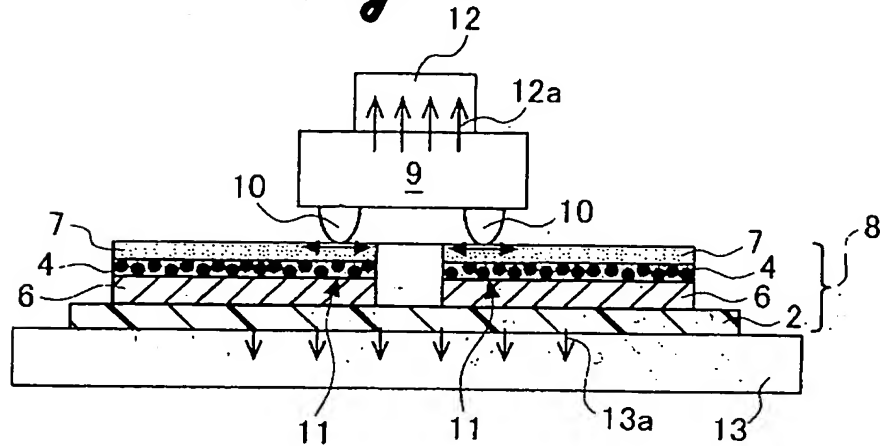


Fig. 3B

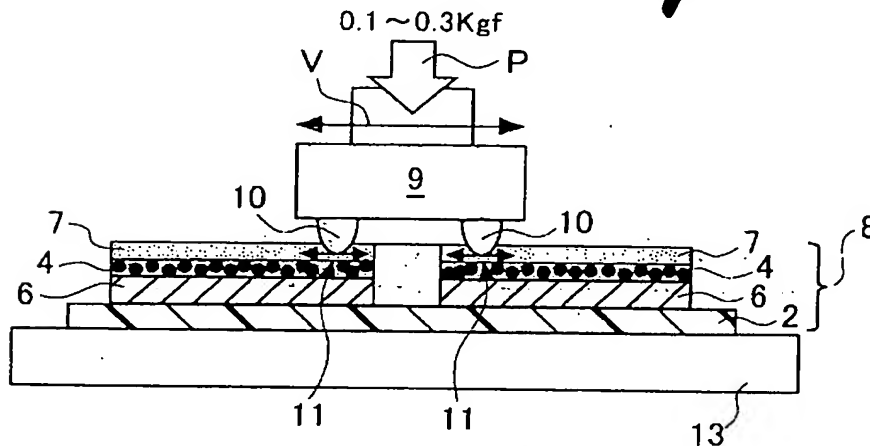


Fig. 3C

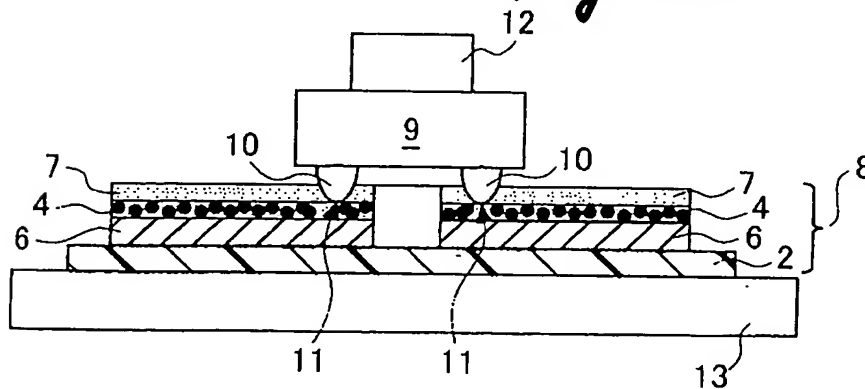


Fig. 4A

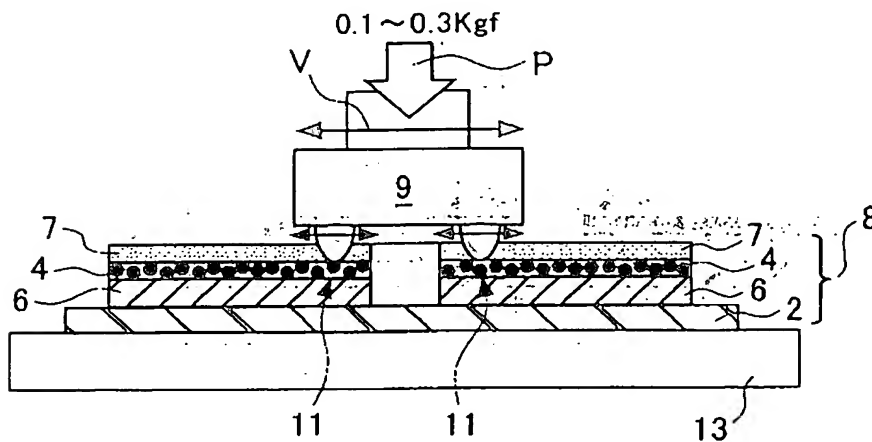


Fig. 4B

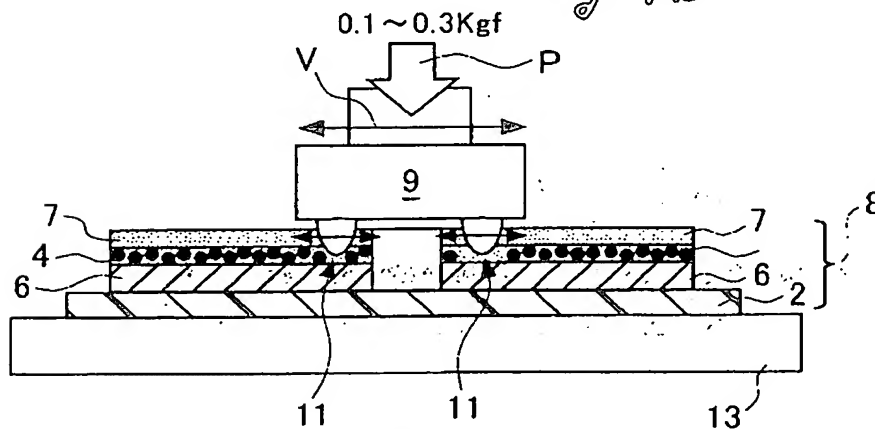


Fig. 4C

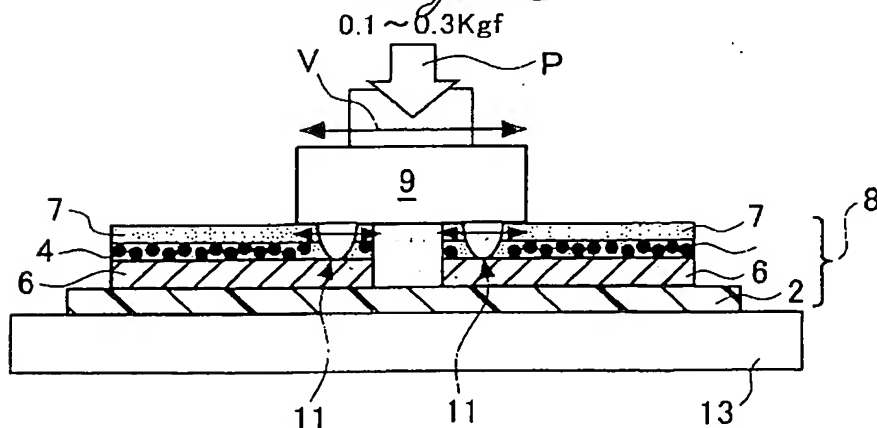


Fig. 5

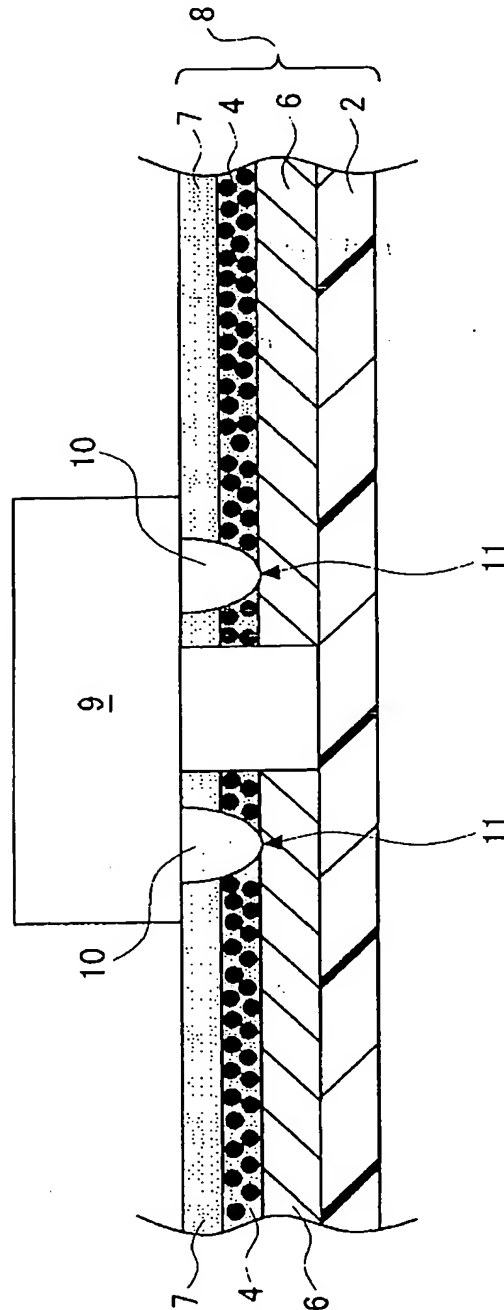


Fig. 6A

<i>Semiconductor Mounting Method</i>	<i>Ultrasonic Bonding</i>	<i>Embodiment</i>
<i>Bonding Strength</i>	<i>200 ~ 250</i>	<i>1400 ~ 1700</i>

Fig. 6B

<i>Semiconductor Mounting Method</i>	<i>Third Method of the related art</i>	<i>Embodiment</i>
<i>Short-Circuit failure Occurrence Ratio</i>	<i>5 . 0%</i>	<i>0 . 0%</i>

Fig. 7A

SiO ₂ Particles	None	Present (Embodiment)
Semiconductor chip bonding failure (100 tests)	96.0%	0.0%

Fig. 7B

SiO ₂ Particles	1~2 μ m	3~4 μ m (Embodiment)
Semiconductor chip bonding failure (100 tests)	50.0%	0.0%

Fig. 8

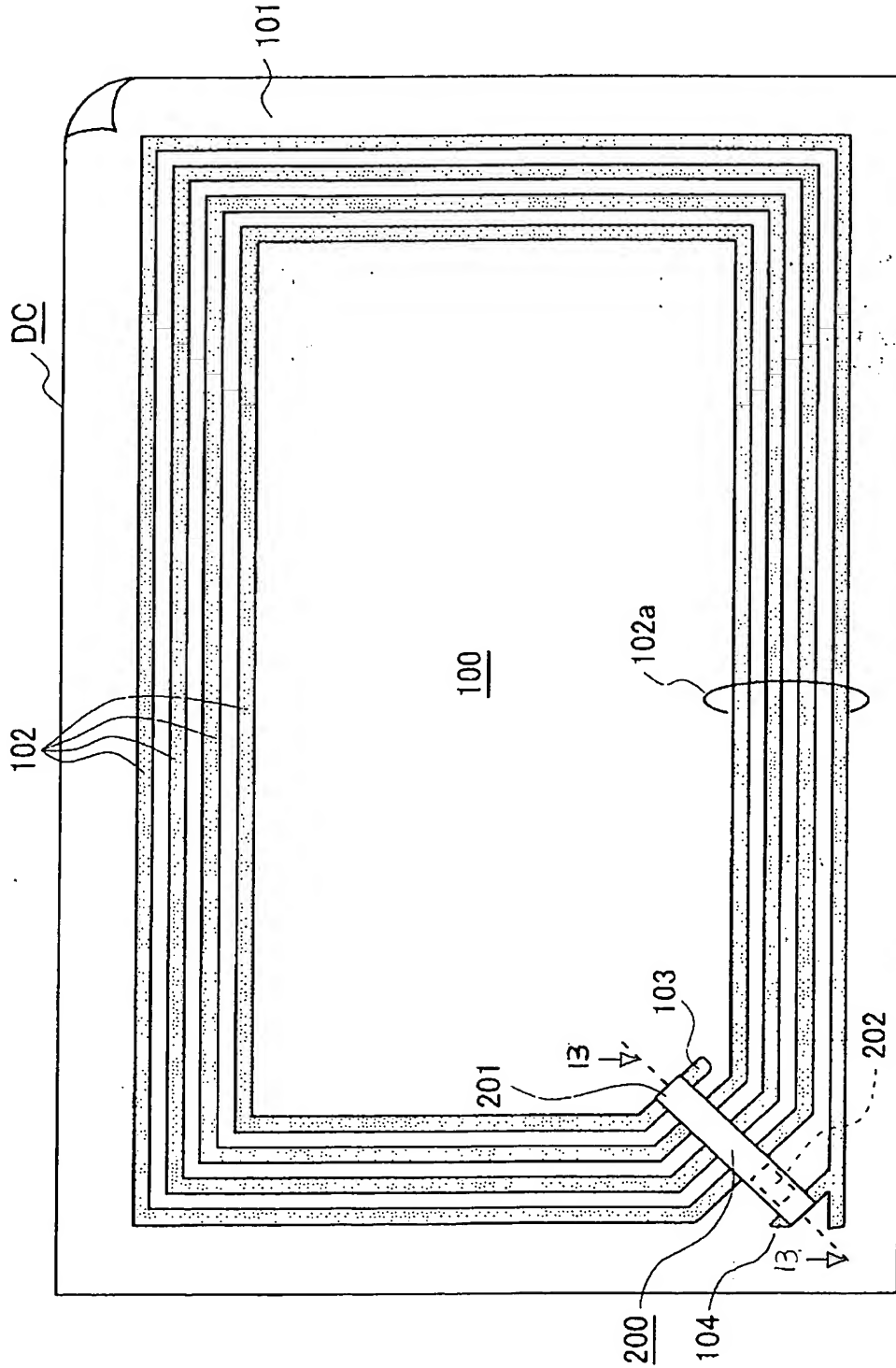


Fig. 9

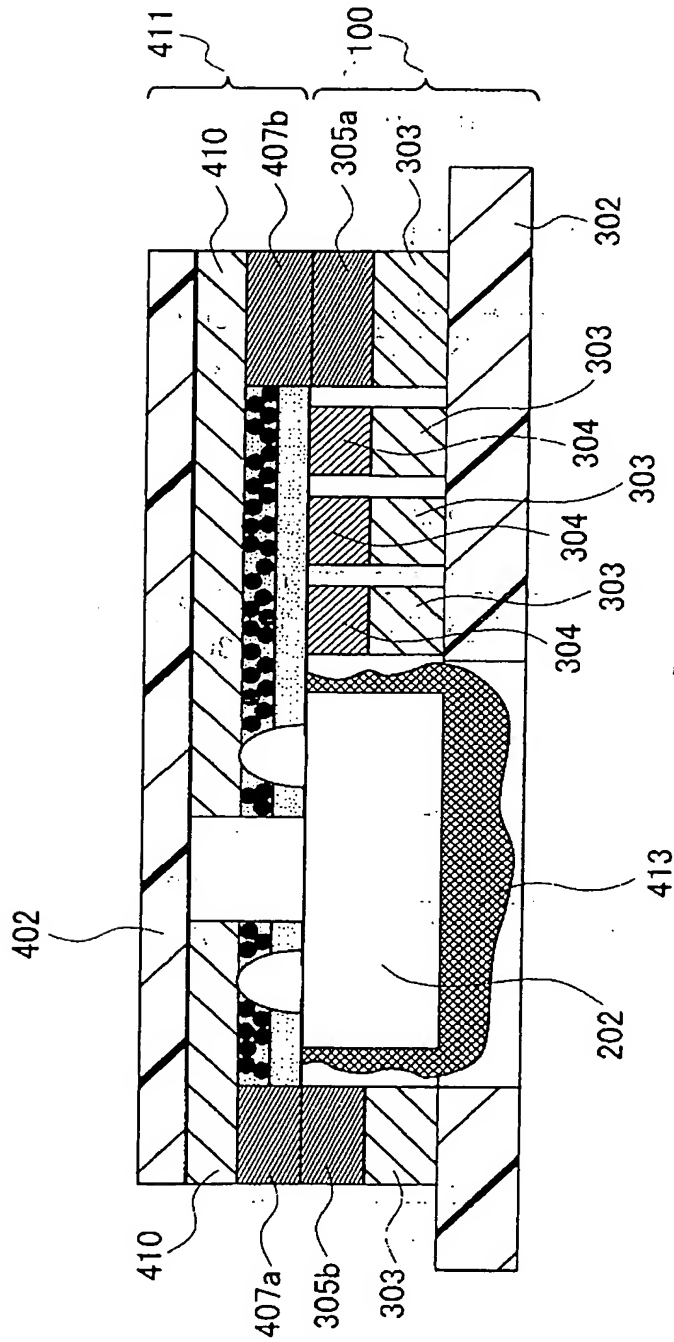


Fig. 10A

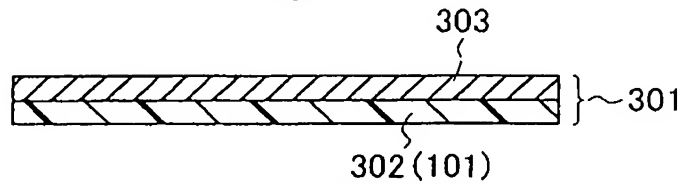


Fig. 10B

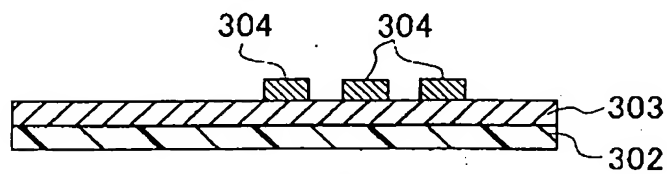


Fig. 10C

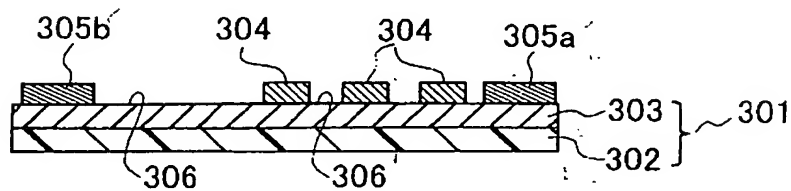


Fig. 10D

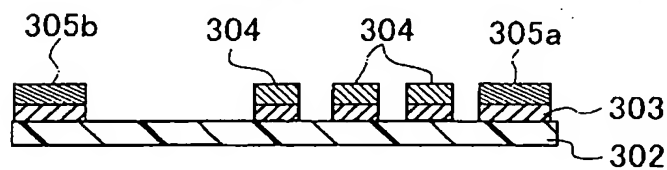


Fig. 10E

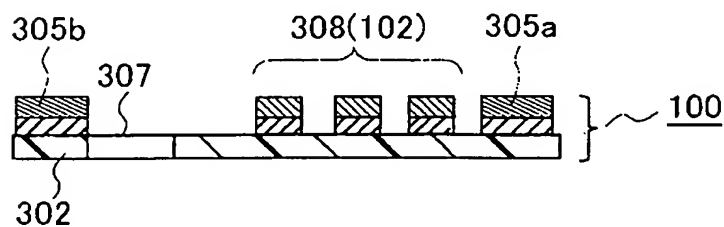


Fig. 11A

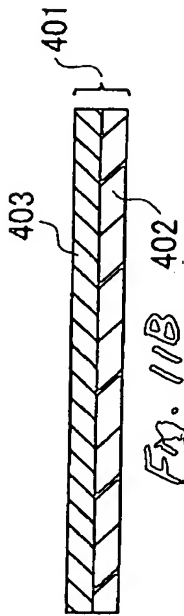


Fig. 11B

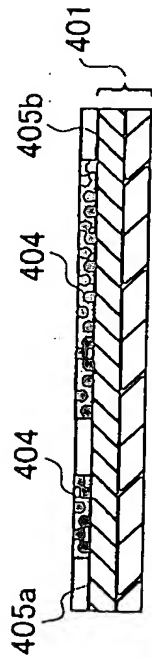


Fig. 11C

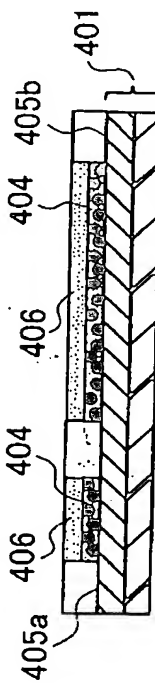


Fig. 11D

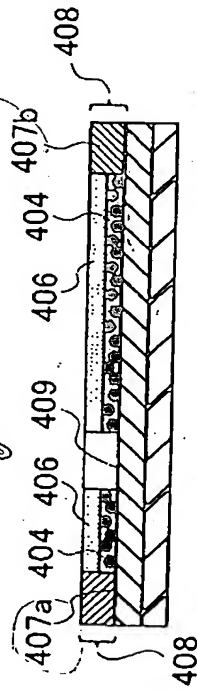


Fig. 11E

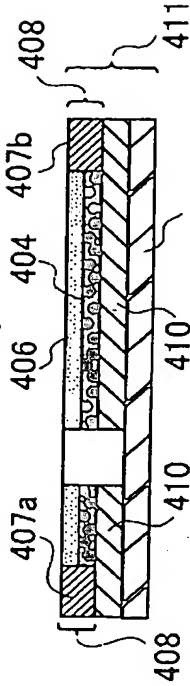


Fig. 11F

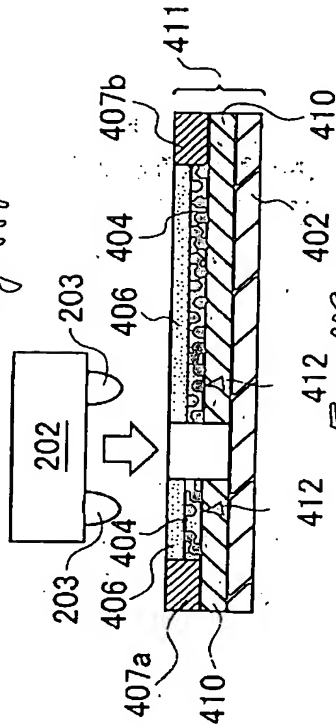


Fig. 11G

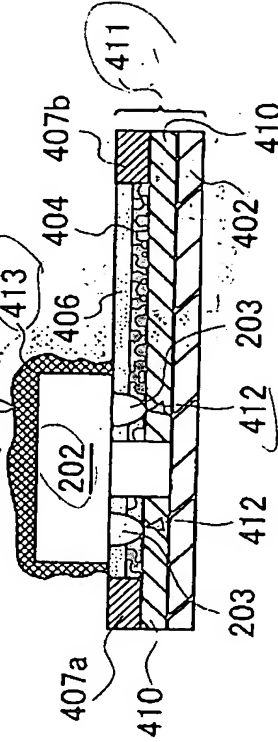


Fig. 12A

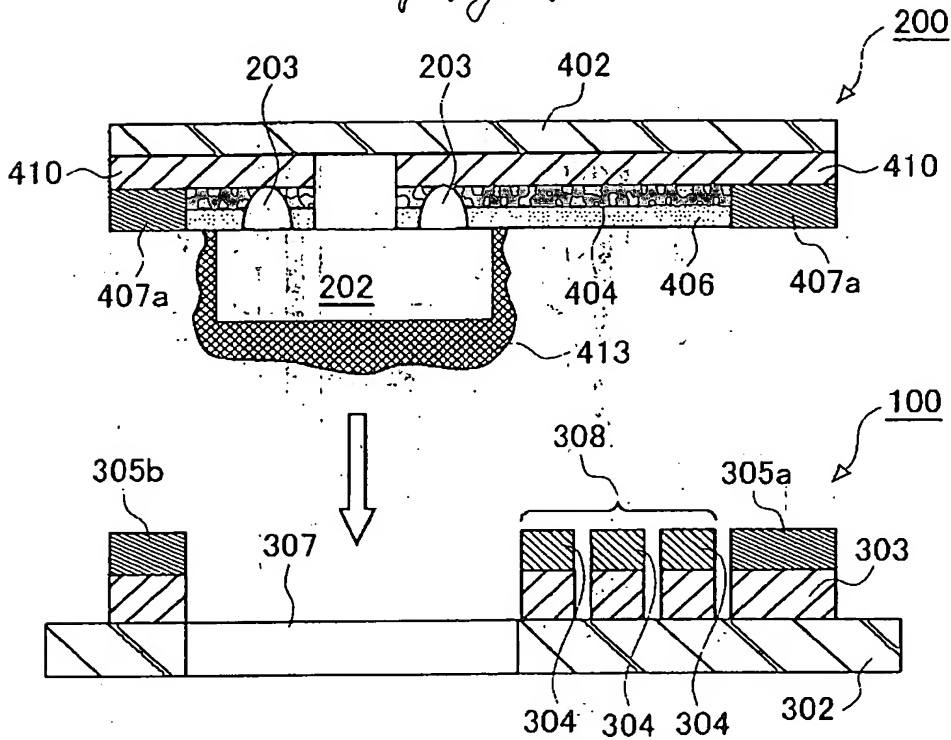


Fig. 12B

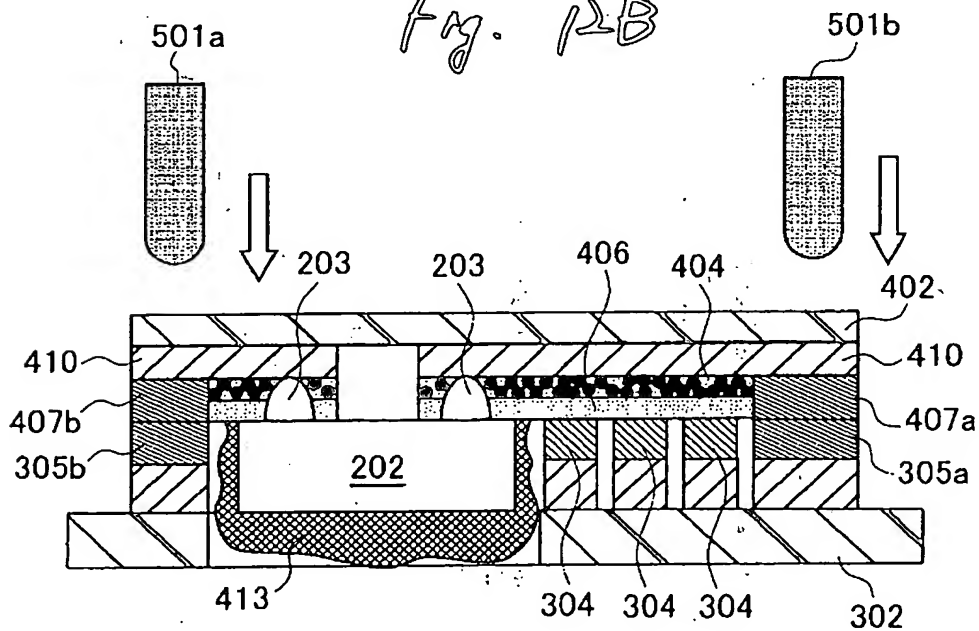


Fig. 13

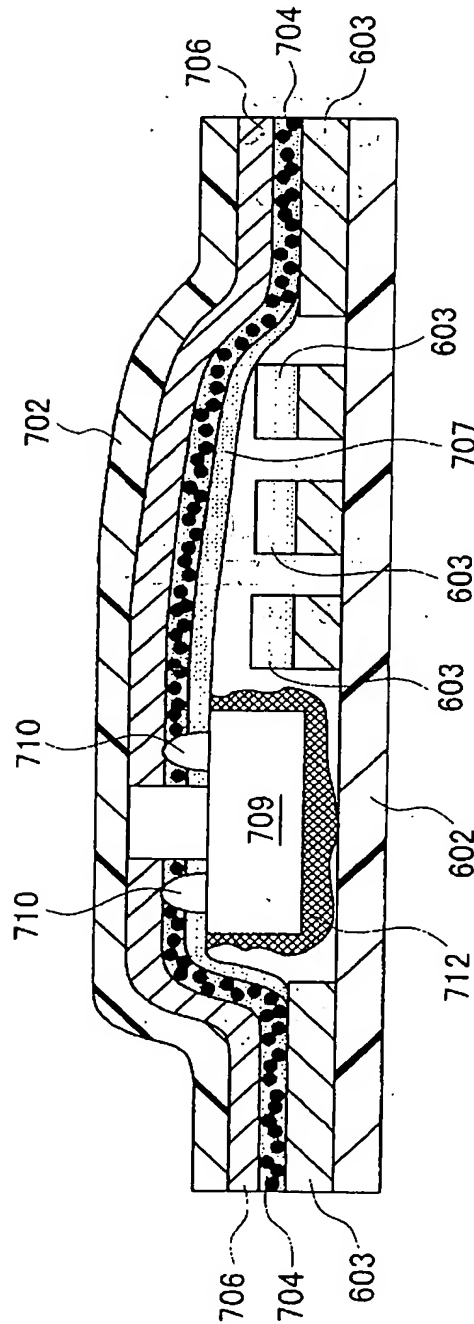


Fig. 14A

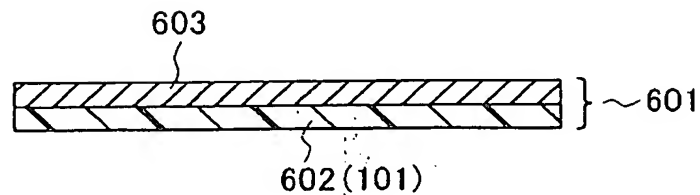


Fig. 14B

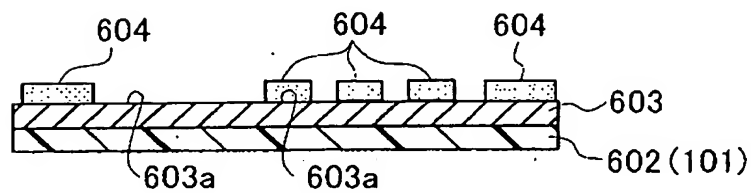


Fig. 14C

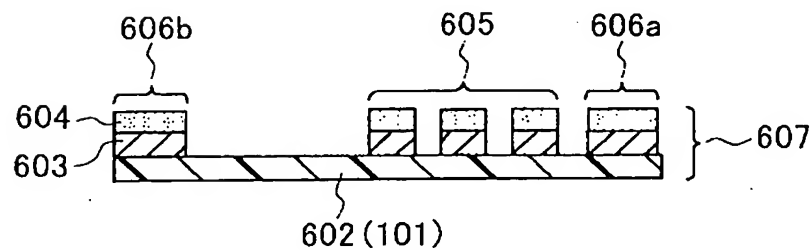


Fig. 15A

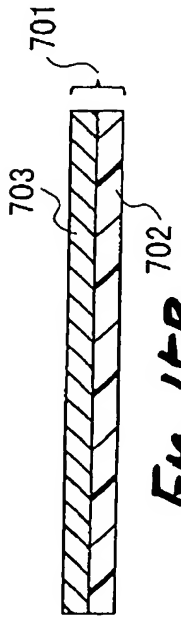


Fig. 15B

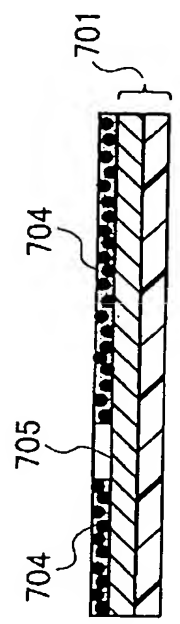


Fig. 15C

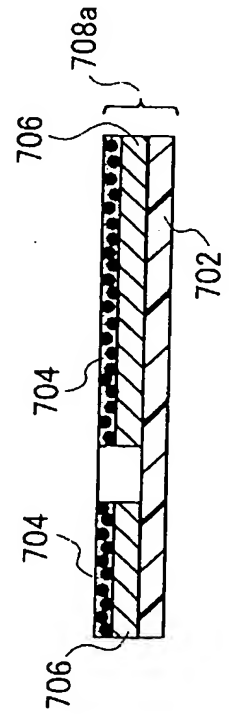


Fig. 15D

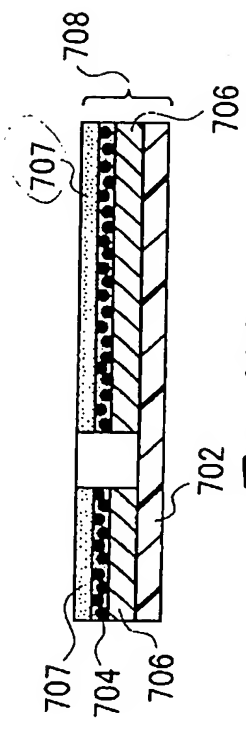


Fig. 15E

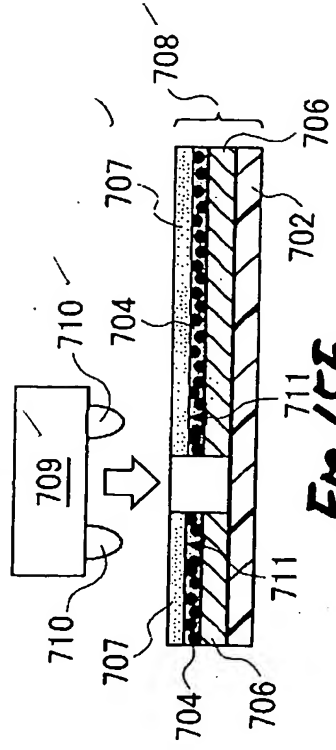


Fig. 15F

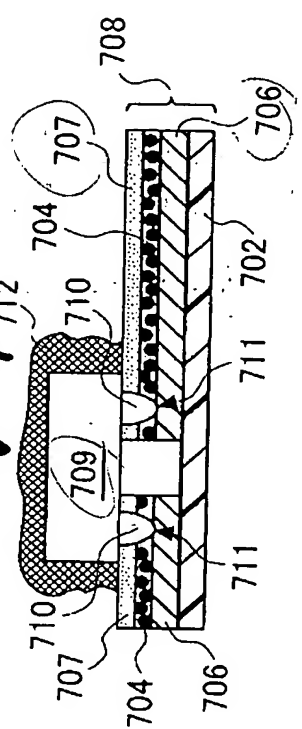


Fig. 16A

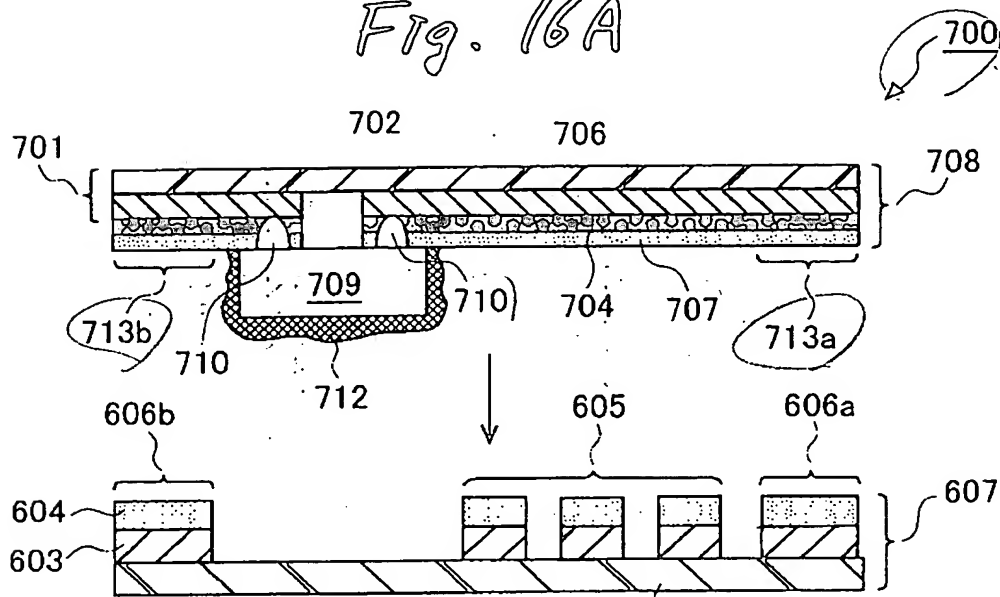


Fig. 16B

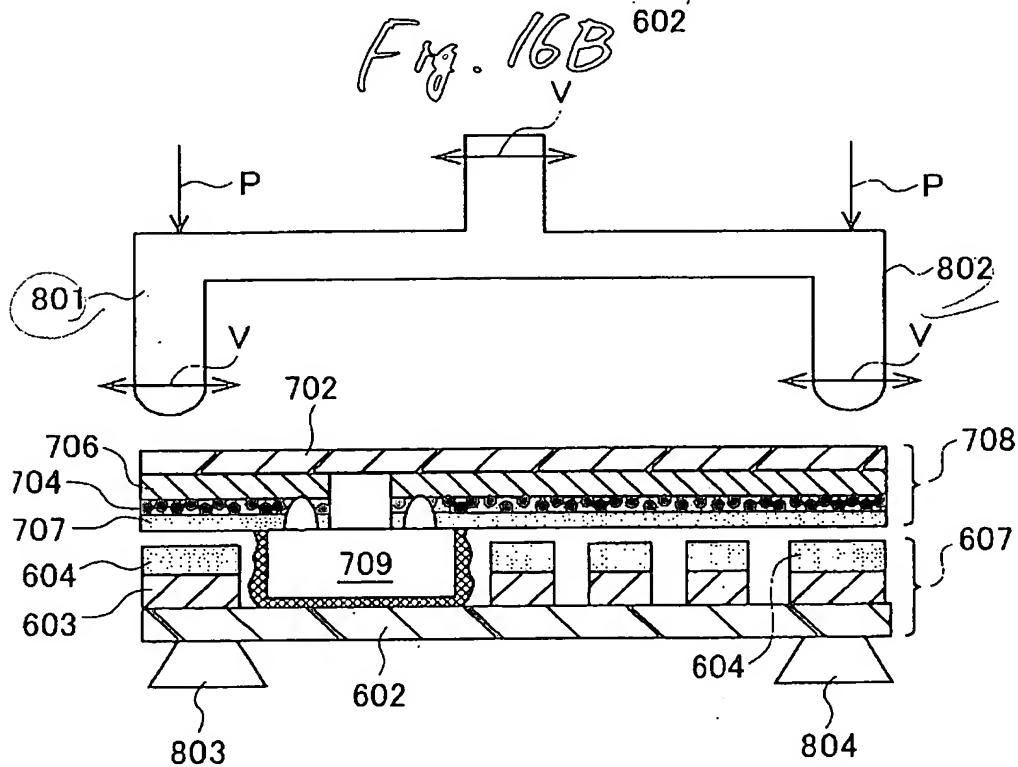


Fig. 17

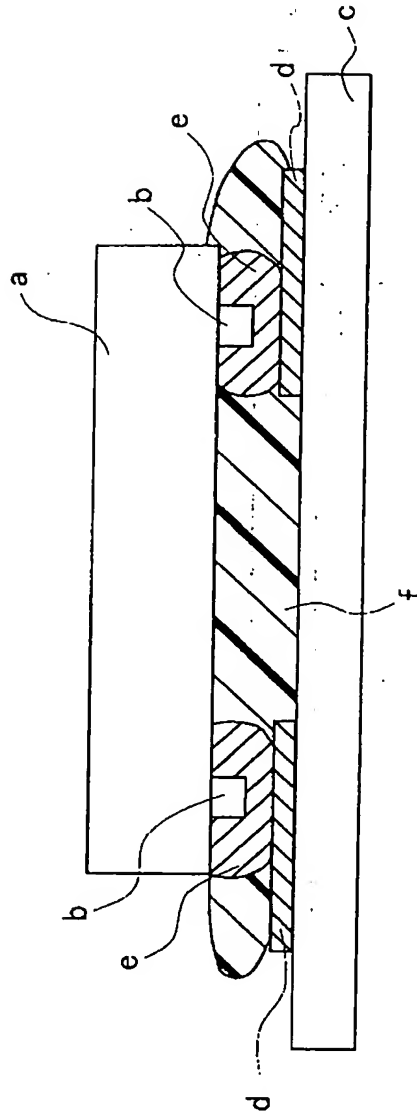


Fig. 18

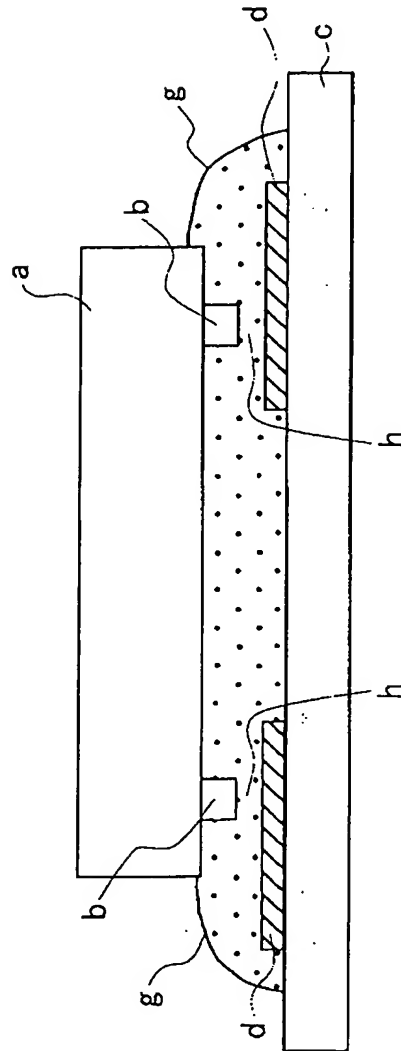


Fig. 19A

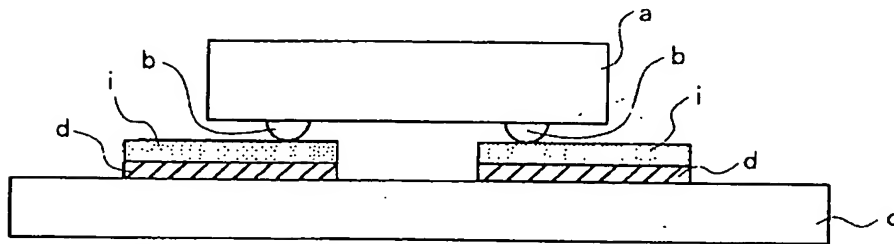


Fig. 19B

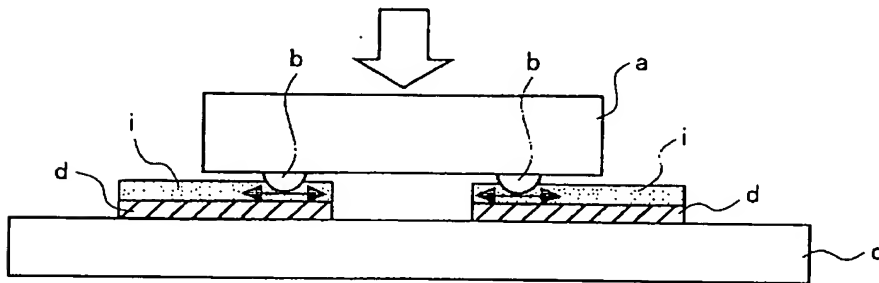


Fig. 19C

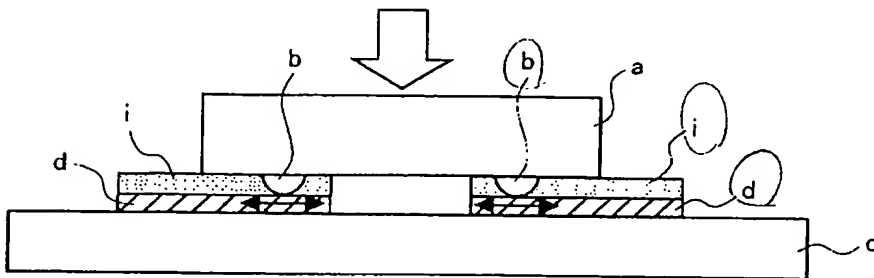


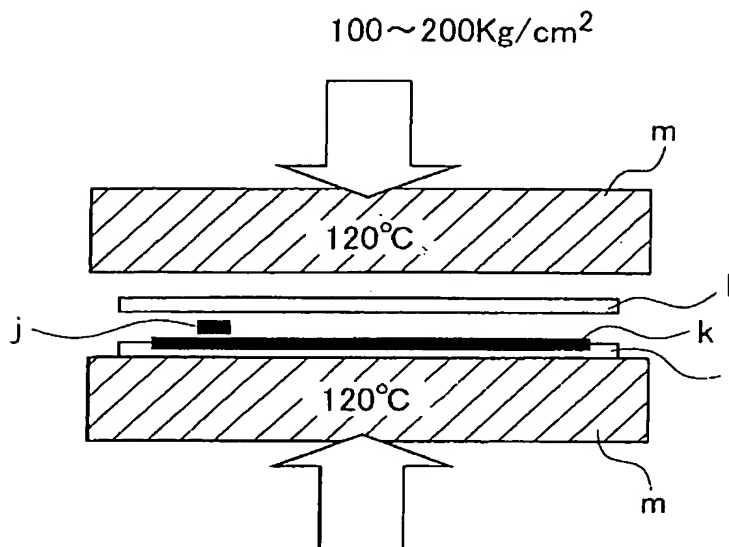
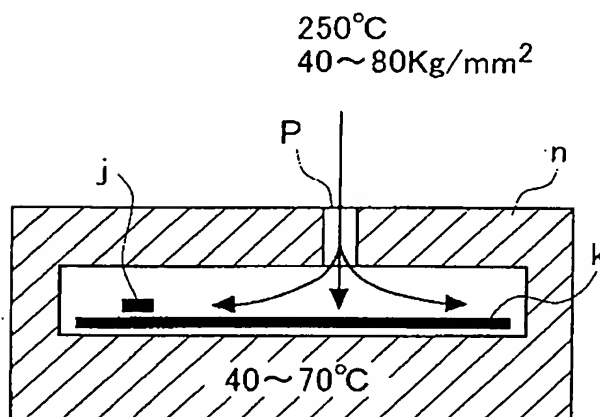
Fig. 20A*Fig. 20B*

Fig. 21A

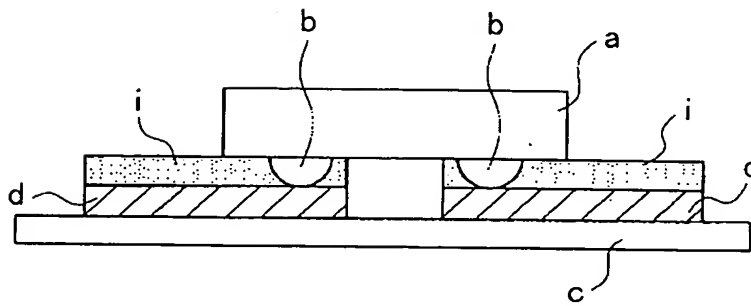


Fig. 21B

